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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,766	01/26/2004	Matthew L. Severson	020417	1936

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EXAMINER	
LUU, AN T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/765,766	SEVERSON, MATTHEW L.	
	Examiner	Art Unit	
	An T. Luu	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7,8,12-16,19-23,26,27,31-35,38,39,44 and 45* is/are rejected.

7)☒ Claim(s) *5,6,9-11,17,18,24,25,28-30,36,37 and 40-43* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because the INPUT CLOCK in figure 5 appears to be pointed to an incorrect direction. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-45 are rejected under 35 U.S.C. 102(b) as being anticipated by the Halter reference (US Patent 6,449,329).

Halter discloses in figure 1 an apparatus comprising a counter (elements 18, 19, 20, 22, 26, 28, 30 and 32) configured to receive the input clock signal (i.e., input of 13) and generate a counter signal (i.e., q1, q2) having a frequency of M cycles for every N cycles of the input signal (col. 1, lines 29-31 and col. 3, lines 10-12); a comparator circuit (24, 34) coupled to the counter to compare a count value D and to generate comparator signals (i.e., pos_edge, neg_edge) related to the comparison; and a control circuit 16 to generate an output clock signal based on the comparator signals as required by claim 1. It is noted that the limitation "to thereby select a rising edge...a falling edge of the input clock signal" is seen as inherent result derived from selecting either inputs (i.e., pos_edge or neg_edge) of the MUX 44.

As to claim 2, col. 4, lines 10-30, disclose the control circuit generates the output clock signal with its rising edge based on a rising edge of the input clock signal if the comparator signals indicate that the counter has a value greater than or equal to zero and less than M/2.

As to claim 3, col. 4, lines 10-30, disclose the control circuit generates the output clock signal with its rising edge based on a falling edge of the input clock signal if the comparator signals indicate that the counter has a value greater than or equal to M/2 and less than M.

As to claim 4, col. 3, lines 29-37, and claim 2 of Halter disclose the counter is a M/N:D counter wherein D is related to a duty cycle of the output clock signal.

As to claims 7 and 8, col. 5, lines 51-53, discloses the control circuit generates the output clock signal with 50% duty cycles in which D=1/2.

As to claim 12, figure 1 discloses the control circuit comprising first and second synchronization latches (36, 38) wherein the first synchronization latch generates the output signal rising edge based on a rising edge of a selected input clock cycle if activated (i.e., by MUX 44), the second synchronization latch generates the output signal rising edge based on a falling edge of an input clock cycle preceding the selected input clock cycle if activated (i.e., by MUX 44).

As to claim 44, the control circuit 16 comprises OR gate to generate selected cycles of the output clock signal with a rising edge based on a rising edge of the input clock signal (i.e., via 36), and selected cycles of the output clock signal with a rising edge of the output clock signal based on a falling edge of the input signal (i.e., via 40).

As to claim 45, the scope of claim is similar to that of claim 44. Therefore, it is rejected for the same reason set forth above. It is noted that positive edge is coupled to latch 38 and negative edge is coupled to latch 36 to achieve the above limitation.

As to claim 13, the scope of claim is similar to that of claim 12. Therefore, it is rejected for the same reason set forth above.

As to claims 14 and 19, the scopes of claims are similar to that of claim 1. Therefore, they are rejected for the same reason set forth above.

As to claims 15 and 16, by virtue of configuration shown in the control circuit 16 (i.e., terminal "1" receives rising edge and terminal "0" receives combined rising and falling signals), the output of the control circuit will generates (1) selected cycles of the output clock signal with a rising edge of the output clock signal based on a rising edge of the input clock and selected cycles of the output clock signal with a rising edge of the output clock signal based on a falling

edge of the input clock or (2) selected cycles of the output clock signal with a falling edge of the output clock signal based on a rising edge of the input clock and selected cycles of the output clock signal with a falling edge of the output clock signal based on a falling edge of the input clock.

As to claim 20, figure 1 discloses counter means 12 and 14 for generating a counter value (q1, q2) based on the input clock signal and comparison means (24 or 34) for comparing the counter value to predetermined count values (i.e., D or M) and output control means 16 for generating the output clock signal with the rising edge of the output clock signal based on a rising edge or a falling edge of the input clock signal and a falling edge of the output clock signal based on a rising edge or a falling edge of the input clock signal based on the comparing by the comparison means.

As to claim 21, col. 4, lines 10-30, disclose the control circuit generates the output clock signal with its rising edge based on a rising edge of the input clock signal if the comparator signals indicate that the counter has a value greater than or equal to zero and less than M/2.

As to claim 22, col. 4, lines 10-30, disclose the control circuit generates the output clock signal with its rising edge based on a falling edge of the input clock signal if the comparator signals indicate that the counter has a value greater than or equal to M/2 and less than M.

As to claim 23, col. 3, lines 29-37, and claim 2 of Halter disclose the counter is a M/N:D counter wherein D is related to a duty cycle of the output clock signal.

As to claims 26 and 27, by virtue of configuration shown in the control circuit 16 (i.e., terminal "1" receives rising edge and terminal "0" receives combined rising and falling signals), the output of the control circuit will generates (1) selected cycles of the output clock signal with

a rising edge of the output clock signal based on a rising edge of the input clock and selected cycles of the output clock signal with a rising edge of the output clock signal based on a falling edge of the input clock or (2) selected cycles of the output clock signal with a falling edge of the output clock signal based on a rising edge of the input clock and selected cycles of the output clock signal with a falling edge of the output clock signal based on a falling edge of the input clock.

As to claims 31-35 38-39, they are rejected for reciting method/step derived from the circuit recited in claims 19-23 and 26-27, which are rejected as noted above.

Response to Arguments

4. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

5. Claims 5, 6, 9-11, 17, 18, 24, 25, 28-30, 36, 37, and 40-43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fails to disclose an apparatus and method thereof comprising elements being configured as recited in claims. Specifically, none of the prior art teaches or fairly suggests, among other things, the following limitations:

- The comparator signals indicate that the counter has a value greater than or equal D and less than D+M/2 as required by claims 5, 24 and 36.
- The comparator signals indicate that the counter has a value greater than or equal D+M/2 and less than D+M as required by claims 6, 25 and 37.
- A mode control input to override the control circuit as required by claims 9, 30 and 42.
- A third comparator as required by claim 10.
- A storage area containing data indicating which of the M cycles of the output clock signal having rising (or falling) edge based on a rising edge of the input clock and which of the M cycles of the output clock signal having rising (or falling) edge based on a falling edge of the input clock as required by claims 17-18, 28-29 and 40-41. And,
- The control circuit is configured to select a rising edge of some cycles of the output clock signal based on a rising edge of the input clock signal, and a rising edge of some other cycles of the output clock signal based on a falling edge of the input clock signal, and to select a falling edge of some cycles of the output clock signal based on a rising edge of the input clock signal, and a falling edge of some other cycles of the output clock signal based on a falling edge of the input clock signal as required by claim 43.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to An T. Luu whose telephone number is 571-272-1746. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

An T. Luu
9-27-05 AL

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